



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/588,617	06/06/2000	Claude L. Bertin	BUR9-1999-0264-US1	1077
30678	7590	09/21/2005	EXAMINER	
CONNOLLY BOVE LODGE & HUTZ LLP SUITE 800 1990 M STREET NW WASHINGTON, DC 20036-3425			NGUYEN, TRUNG Q	
			ART UNIT	PAPER NUMBER
			2829	

DATE MAILED: 09/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

<b>Office Action Summary</b>	Application No. 09/588,617	Applicant(s) BERTIN ET AL.	
	Examiner Trung Q. Nguyen	Art Unit 2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 30 June 2005.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-7, 11-15, 21-26, 30 and 31 is/are pending in the application.  
4a) Of the above claim(s) 8-10, 16-20 and 27-29 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-7, 11-15, 21-26, 30 and 31 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-7, 11-15 and 21-26 and 30-31 are rejected under 35 U.S.C. 102(e) as being anticipated by Hembree (U.S. 6,504,389).

Regarding claim 1, Hembree discloses in Figs. 4A –B a plurality of semiconductor devices 44, a device carrier 46-48, carrier having interconnect wiring 52 and 94 therein sufficient for both operational testing and packaging of semiconductor devices 44; attaching semiconductor devices 44 to carrier 46-48 (see Fig. 4B); testing devices via wiring 60 and 62 of Fig. 4A; and dividing carrier into a plurality of components wherein each component contains at least one semiconductor device (Fig. 4B wherein semiconductor device 44 placing in different spots).

Regarding claims 2-3, Hembree discloses in Figs. 4A –C installing one component on a next level of assembly (semiconductor device 44 placed in carrier 48 and install component 42 without separating device from carrier 46-48).

Regarding claim 4, Hembree discloses in Fig. 8A the printed circuit board included in carrier 46-48.

Regarding claims 5, 14 and 31, Hembree discloses in Figs. 4A and 6, wherein semiconductor device 104 comprising leads (portion of 120) and wherein carrier 46-48 comprising contacts for external connection 52 of Fig. 4A.

Regarding claims 6-7 and 11-12, Hembree discloses in Figs. 4A and 6 wherein lead reduction mechanism (connection between lead 120 of semiconductor device 104 of Fig. 6 and external connection 52 of Fig. 4A) comprising a built in self-test engine 58-62 of Fig. 4A.

Regarding claim 13, Hembree discloses in Figs. 4A running semiconductor devices 44 in carrier 46-48 (see Fig. 4B); testing devices via wiring 60 and 62 of Fig. 4A; and dividing carrier into a plurality of components via independently and simultaneously.

Regarding claims 14-15 Hembree discloses in Figs. 4A-B attaching semiconductor devices 44 to carrier 46-48 (see Fig. 4B); testing devices via wiring 60 and 62 of Fig. 4A; and dividing carrier into a plurality of components wherein each component contains at least one semiconductor device (Fig. 4B wherein semiconductor

Art Unit: 2829

device 44 placing in different spots); and dividing carrier into separate multi-chip final assemblies 42 of Fig. 4B

Regarding claims 21-22, Hembree discloses in Figs. 4A-B wherein carrier comprises connectors 94, 52 and 58 on two sides of carrier (see Fig. 4A) and encapsulating semiconductor devices 44 via cap 55 or 88.

Regarding claims 23-26, Hembree discloses in column 12, lines 16-38, wherein the system identifying, repair and remove defective semiconductor devices.

Regarding claim 30, Hembree discloses in Figs. 4A –B a device carrier 46-48 wherein carrier having interconnect wiring therein 10, 94 and 58 for testing and packaging, a plurality of semiconductor devices 44, carrier having interconnect wiring 52 and 94 therein sufficient for both operational testing and packaging of semiconductor devices 44; attaching semiconductor devices 44 to carrier 46-48 (see Fig. 4B); testing devices via wiring 60 and 62 of Fig. 4A; and dividing carrier into a plurality of components wherein each component contains at least one semiconductor device (Fig. 4B wherein semiconductor device 44 placing in different spots).


### ***Conclusion***

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Trung Nguyen** whose telephone number is **(571) 272-**

Art Unit: 2829

**1966.** The examiner can normally be reached on Monday through Friday, 8:30AM – 5:00PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **RAMIREZ NESTOR** can be reached at **(571)-272-2034**.

**Trung Nguyen**  
Patent Examiner  
Group Art Unit 2829  
September 13, 2005

  
**VINH NGUYEN**  
**PRIMARY EXAMINER**  
A.U. 2829  
09/15/05